AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A method comprising:

interfacing a first device with a second device;

clocking at least a portion of the second device with a first clock signal;

transmitting a clock signal source from the second device to the first device;

transmitting a second clock signal from the first device to the second device,

wherein the second clock signal ~~being~~ is the clock signal source delayed by a propagation delay;

adjusting a phase of the clock signal source such that a phase of the second clock signal is substantially in alignment with a phase of the first clock signal; and

transmitting data clocked by the second clock signal from the first device to the second device.

2. (Original) The method of claim 1, wherein the second device is a high speed analog semiconductor device.

3. (Original) The method of claim 1, wherein the first device is a CMOS semiconductor device.

4. (Original) The method of claim 1, wherein the phase of the clock signal source is adjusted by modifying the frequency of the clock signal source.

5. (Original) The method of claim 1, wherein the data is transmitted from the second device to the first device without an initiation sequence.

6. (Original) The method of claim 1, further comprising receiving a reference clock signal, wherein the first clock signal and the clock signal source are generated from the reference clock signal.

7. (Original) The method of claim 1, further comprising reducing a frequency of the clock signal source if a frequency of the second clock signal is less than the frequency of the clock signal source.

8. (Currently amended) A transmitter comprising:

a subpart that is clocked by a first clock signal;

a first interface connection to a device, the device transmitting data to the transmitter using the first interface connection;

a second interface connection to the device, the transmitter ~~transmitting~~ transmit a clock signal source to the device using the second interface connection;

a third interface connection to the device, the device transmitting a second clock signal to the transmitter using the third interface connection, wherein the second clock signal ~~being~~ is the clock signal source delayed by a propagation delay through a portion of the device; and

a phase detection unit, the phase detection unit adjusting the phase of the clock signal source to align the phase of the second clock signal with the phase of the first clock signal.

9. (Currently amended) The transmitter of claim 8, further comprising a reference clock signal connection, the transmitter ~~receiving~~ to receive a reference clock signal using the reference clock connection.

10. (Currently amended) The transmitter of claim 9, further comprising a clock multiplier unit, the transmitter ~~using~~ to use the clock multiplier unit to generate the first clock signal and the clock signal source from the reference clock signal.

11. (Original) The transmitter of claim 8, wherein the phase detection unit adjusts the phase of the clock signal source by adjusting the frequency of the clock signal source.

12. (Original) The transmitter of claim 8, wherein the transmitter reduces a frequency of the clock signal source if a frequency of the second clock signal is less than the frequency of the clock signal source.

13. (Original) The transmitter of claim 8, wherein the phase detection unit is a set-reset latch based phase frequency detector.

14. (Currently amended) A self-synchronizing interface comprising:

a first interface connection between a first device and a second device, the second device transmitting a ~~first~~ clock signal source to the first device through the first interface connection;

a second interface connection between the first device and the second device, the first device transmitting a first clock signal that is a delayed version of the ~~first~~ clock signal source to the second device, the second device modifying

the phase of the ~~first~~ clock signal source such that the phase of the ~~delayed version of the~~ first clock signal aligns with the phase of a second clock signal, wherein at least a portion of the second device ~~being~~ is clocked by the second clock signal; and

a third interface connection between the first device and the second device, the first device transmitting data to the second device through the third interface connection, wherein the data ~~being~~ is clocked by the delayed version of the first clock signal.

15. (Currently amended) The interface of claim 14, wherein the second device modifies the phase of the ~~first~~ clock signal source by modifying the frequency of the first clock signal.

16. (Original) The interface of claim 14, wherein the second device reduces a frequency of the first clock signal source if a frequency of the delayed version of the first clock signal is less than a frequency of the clock signal source.

17. (Currently amended) A data communication system comprising;

a first subsystem, the first subsystem receiving a ~~first~~ clock signal source, the first subsystem further transmitting data that is clocked by a ~~second~~ first clock signal, the ~~second~~ first clock signal being the ~~first~~ clock signal source delayed by a propagation delay through at least a portion of the first subsystem; and

a second subsystem, the second subsystem transmitting the ~~first~~ clock signal source to the first subsystem and receiving the data and the ~~second~~ first

clock signal from the first subsystem, at least a portion of the second subsystem being clocked by a ~~third~~ second clock signal, the second subsystem modifying the phase of the ~~first~~ clock signal source to align the phase of the ~~second~~ first clock signal with the phase of the ~~third~~ second clock signal.

18. (Original) The data communications system of claim 17, wherein the first subsystem includes a buffer memory.

19. (Original) The data communications system of claim 17, wherein the second subsystem operates at a higher speed than the first subsystem.

20. (Currently amended) The data communications system of claim 17, wherein the second subsystem modifies the phase of the ~~first~~ clock signal source by modifying the frequency of the ~~first~~ clock signal source.

21. (Currently amended) The data communications system of claim 17, wherein the second subsystem reduces the frequency of the ~~first~~ clock signal source if the frequency of the ~~second~~ first clock signal is below the frequency of the ~~first~~ clock signal source.

22. (Original) The data communications system of claim 17, wherein the second subsystem includes a phase frequency detector.

23. (Original) The data communications system of claim 22, wherein the phase frequency detector is a set-reset latch based phase frequency detector.

24. (Currently amended) A method comprising:

interfacing a first device with a second device;

generating a first clock signal and a ~~second~~ clock signal source;

clocking at least a portion of the second device with the first clock signal;

transmitting the ~~second~~ clock signal source from the second device to the first device;

generating a ~~third~~ second clock signal, wherein the third clock signal ~~being~~ is the ~~second~~ clock signal source after propagating through a portion of the first device;

transmitting the ~~third~~ second clock signal and data clocked by the ~~third~~ second clock signal from the first device to the second device;

detecting phases and frequencies of the first clock signal and the ~~third~~ second clock signal and comparing the phase of the first clock signal to the phase of the ~~third~~ second clock signal; and

if the phase of the first clock signal and the phase of the ~~third~~ second clock signal are not in alignment, modifying the phase of the ~~second~~ clock signal source until the phase of the ~~third~~ second clock signal is aligned with the phase of the first clock signal.

25. (Currently amended) The method of claim 24, further comprising reducing a frequency of the ~~second~~ clock signal source if the frequency of the ~~third~~ second clock signal is below the frequency of the ~~second~~ clock signal source.

26. (Currently amended) The method of claim 25, wherein the frequency of the ~~third~~ second clock signal is below the frequency of the ~~second~~ clock signal source

because the frequency of the ~~second~~ clock signal source is above a maximum frequency that can be generated by the first device.

Please add the following claims:

27. (New) A method comprising:

coupling a first device with a second device;

clocking at least a portion of the second device with a first clock signal;

transmitting a clock signal source from the second device to the first device;

transmitting a second clock signal from the first device to the second device, wherein the second clock signal is the clock signal source delayed by a propagation delay;

detecting a difference between a phase of the first clock signal and a phase of the second clock signal;

adjusting a phase of the clock signal source to align the phase of the second clock signal with the phase of the first clock signal; and

transmitting data clocked by the second clock signal from the first device to the second device.

28. (New) The method of claim 27, wherein adjusting the phase of the clock signal source comprises modifying the frequency of the clock signal source.

29. (New) The method of claim 27, further comprising reducing a frequency of the clock signal source if a frequency of the second clock signal is less than the frequency of the clock signal source.